DATA SHEET

TDA8050A
QPSK transmitter

Product specification
File under Integrated Circuits, IC02

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Philips
Semiconductors

PHILIPS

QPSK transmitter TDA8050A

FEATURES

- Programmable gain
- PLL controlled carrier frequency
- 3-wire transmission bus
- 5 V supply voltage.

APPLICATIONS

- QPSK modulation.

GENERAL DESCRIPTION

The Quadrature Phase Shift Keying (QPSK) transmitter IC is a monolithic bipolar IC dedicated to quadrature modulation of the I and Q signals. It includes:

- Two double balanced mixers
- A balanced voltage controlled oscillator (VCO) with 0 to 90 degrees signal generation for modulation
- A phase locked loop (PLL) for IF frequency control
- A conversion mixer
- A PLL for RF frequency control
- A gain controlled output amplifier
- A 3-wire bus and an output buffer.

Two PLLs are incorporated, the first PLL includes:

- A fixed main divider
- A crystal oscillator and its programmable reference divider
- A phase/frequency detector, combined with a fixed charge pump.

The second PLL includes:

- A divide-by-four preamplifier
- A 12-bit programmable divider
- A crystal oscillator and its programmable reference divider
- A phase/frequency detector, combined with a programmable charge pump which drives the tuning amplifier, including 30 V output.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage	4.75	5.00	5.25	V
f_c	output centre frequency	5	–	65	MHz
$V_{o(max)}$	maximum output level	–	55	–	dBmV
f_{xtal}	crystal frequency	1	–	4	MHz
$f_{ref(MOD)}$	reference frequency for modulator synthesizer	–	250	–	kHz
f_{step}	frequency step size for converter synthesizer	100	–	500	kHz
T_{amb}	ambient temperature	0	–	70	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8050A	SO32	plastic small outline package; 32 leads; body width 7.5 mm	SOT287-1

BLOCK DIAGRAM

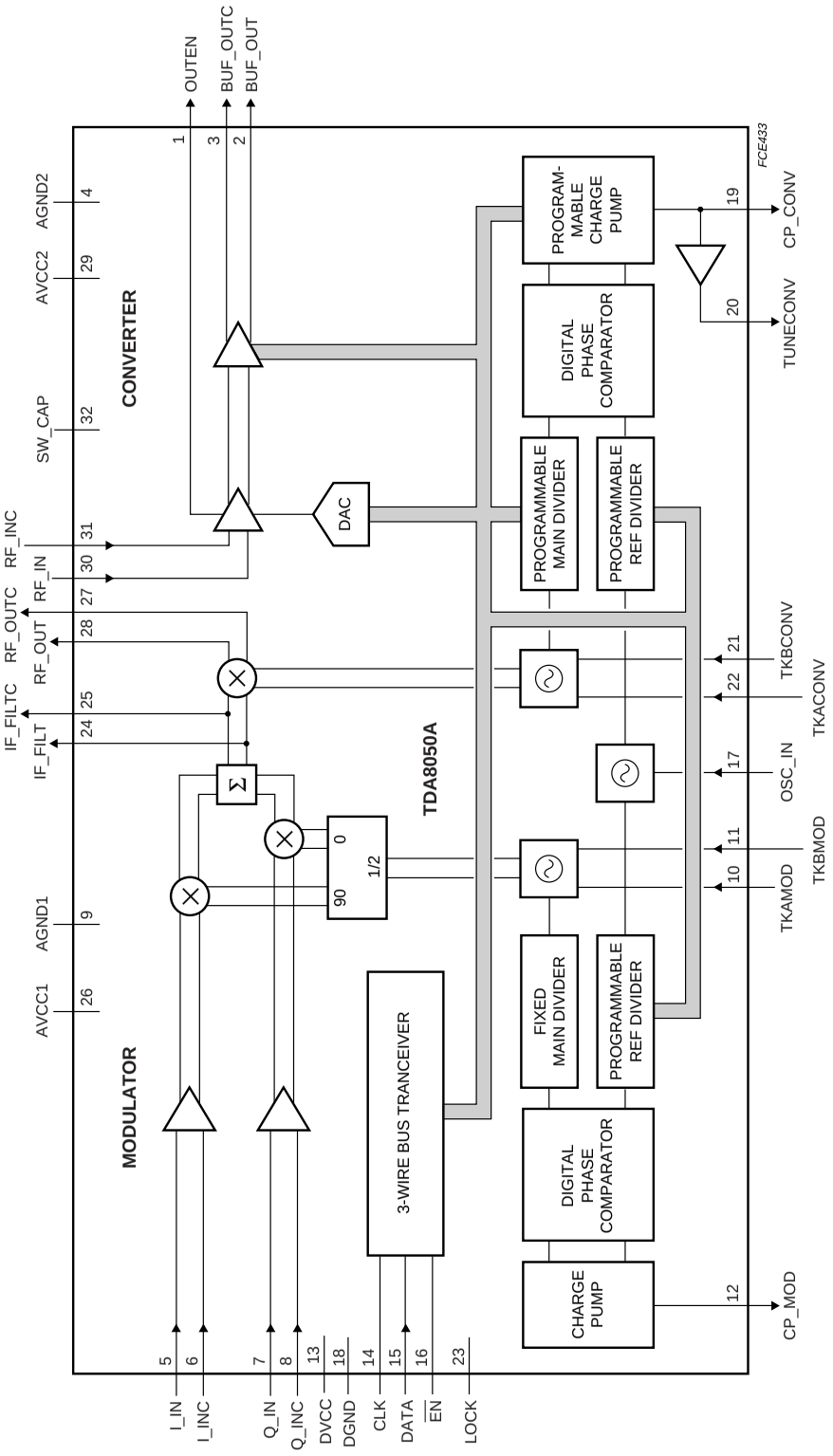


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
OUTEN	1	output enable
BUF_OUT	2	output amplifier balanced output
BUF_OUTC	3	output amplifier balanced output
AGND2	4	converter analog ground 2
I_IN	5	I balanced input
I_INC	6	I balanced input
Q_IN	7	Q balanced input
Q_INC	8	Q balanced input
AGND1	9	modulator analog ground 1
TKA_MOD	10	modulator VCO tank circuit input 2
TKB_MOD	11	modulator VCO tank circuit input 1
CP_MOD	12	modulator charge pump output for PLL loop filter
V_{CCD}	13	digital supply voltage
CLK	14	3-wire bus serial control clock
DATA	15	3-wire bus serial control data
$\overline{EN}$	16	3-wire bus serial control enable
OSC_IN	17	crystal oscillator input
DGND	18	digital ground
CP_CONV	19	converter charge pump output for PLL loop filter
TUNE_CONV	20	tuning voltage output for converter VCO
TKB_CONV	21	converter VCO tank circuit input 1
TKA_CONV	22	converter VCO tank circuit input 2
LOCK	23	lock detect signal
IF_FILT	24	IF balanced output to filter
IF_FILTC	25	IF balanced output to filter
V_{CCA1}	26	modulator analog supply voltage
RF_OUTC	27	RF balanced output to filter
RF_OUT	28	RF balanced output to filter
V_{CCA2}	29	converter analog supply voltage
RF_IN	30	RF balanced input to programmable amplifier
RF_INC	31	RF balanced input to programmable amplifier
SW_CAP	32	switch capacitor

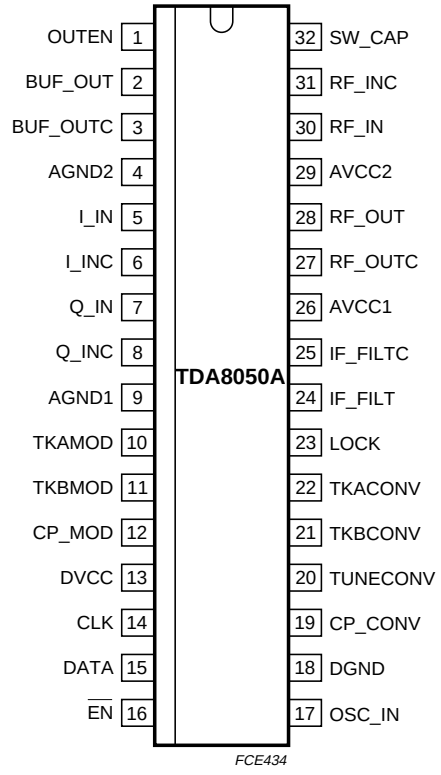


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The I and Q signals are balanced analog signals of 400 mV (p-p). These are mixed by two double balanced mixers with the output signal generated by a first local oscillator, to provide the modulated signal.

The modulated signal is then filtered by an IF filter. This filtered signal, together a signal generated by a second local oscillator, is converted by a balanced mixer to produce the QPSK signal.

The QPSK signal is amplified by a gain controlled output amplifier to a level suitable for transmission. The gain of the amplifier is bus controlled and this amplifier can be disabled when not transmitting, to provide signal attenuation.

The amplified signal is applied to an on-chip amplifier with two balanced outputs (open collector) connected to two off-chip resistors (values 150 Ω), in turn connected to 9 V. The balanced outputs drive a 2 : 1 transformer (Siemens V944) loaded with 75 Ω, which gives an output level of 55 dBmV. The output frequency range of the transmitter is 5 to 65 MHz.

The frequency of the first local oscillator operates at twice the frequency (i.e. 280 MHz), fixed by a PLL implemented in the circuit.

The frequency of the second local oscillator operates in the 145 to 205 MHz bandwidth and can be programmed through the PLL implemented in the circuit.

The VCOs of both the first and second local oscillators need an external LC tank circuit with two varicap diodes.

The data sent to the PLL is loaded in bursts framed by signal $\overline{EN}$. Programming rising clock edges and their appropriate data bits are ignored until $\overline{EN}$ goes active (LOW). The internal latches are updated with the latest programming data when $\overline{EN}$ returns to inactive (HIGH). Only the last 14 bits are stored in the programming register.

No check is made on the number of clock pulses received during the time that programming is enabled. If $\overline{EN}$ goes high while CLK is still LOW, a wrong active clock edge will be generated, causing a shift of the data bits. At power up, $\overline{EN}$ should be HIGH. The lock detector output LOCK is HIGH when both PLLs are in lock.

The main divider ratio and the reference divider ratios are provided via the serial bus. A control register controls the Digital-to-Analog-Converter (DAC), the output amplifier and the charge pump currents (see Tables 1, 2 and 3).

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CC}	supply voltage	–0.3	+6.0	V
t_{sc}	short-circuit time (every pin to V_{CC} or GND)	–	10	s
V_{MAX}	voltage on all pins except BUF_OUT, BUF_OUTC and TUNE_CONV	–0.3	V_{CC}	V
$V_{o(tune)}$	output tuning voltage	–0.3	+30	V
$V_{O(buf)}$	output buffer voltage on pins BUF_OUT and BUF_OUTC	–	10	V
P_{tot}	maximum power dissipation	–	940	mW
T_{amb}	ambient temperature	0	70	°C
T_{stg}	storage temperature	–40	+150	°C
$T_{j(max)}$	maximum junction temperature	–	150	°C

HANDLING

Human Body Model (HBM): The IC pins withstand 2 KV, except pins 27 and 28 (1750 V).
Machine Model (MM): The IC pins withstand 100 V.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	63	K/W

CHARACTERISTICS

Measured in application circuit with the following conditions; V_{CC} = 5 V, T_{amb} = 25 °C; all AC units are RMS values, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{CCA1}	modulator analog supply voltage		4.75	5	5.25	V
I_{CCA1}	modulator analog supply current		33	39	45	mA
V_{CCA2}	converter analog supply voltage		4.75	5	5.25	V
I_{CCA2}	converter analog supply current		39	47	55	mA
$I_{CC(buf)}$	buffer output supply current		39	43	47	mA
V_{CCD}	digital supply voltage		4.75	5	5.25	V
I_{CCD}	digital supply current		20.5	23.5	26.5	mA
$V_{CC(tune)}$	tuning supply voltage		–	–	30	V

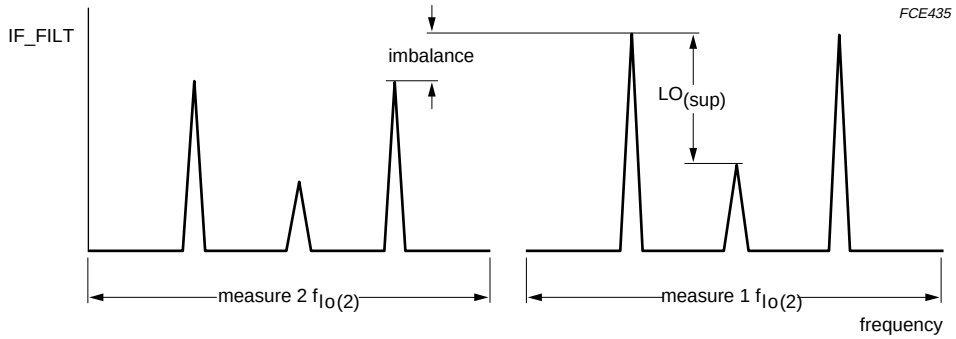
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Quadrature modulator						
I and Q inputs						
$V_{i(DC)}$	input DC level		–	$0.5 \times V_{CC}$	–	V
$V_{i(p-p)}$	signal input level (balanced) (peak-to-peak)	indicative	–	400	500	mV
$f_{i(max)}$	I and Q maximum input frequency	indicative	–	10	–	MHz
$Z_{i(dif)}$	differential input impedance		–	4.4	–	kΩ
$B_{(1\ dB)}$	1 dB bandwidth amplifier	indicative	–	10	–	MHz
Modulator						
f_c	output centre frequency		–	–	140	MHz
ΔA	amplitude imbalance	see Fig.3	–	–	±1	dB
$\Delta\Phi$	phase imbalance		–	–	±2	deg
$LO_{(sup)}$	LO suppression	see Fig.3	–	–28	–	dBc
$Z_{o(dif)}$	differential output impedance		–	1.8	–	kΩ
Modulator VCO						
$F_{OSC(mod)}$	oscillation frequency		–	–	280	MHz
Converter output						
V_O	output level	f = 5 MHz; V_i = 100 mV_{dif} at I and Q inputs	37.5	40	42.5	dBmV
ΔV_O	output flatness	f = 5 to 65 MHz; V_i = 100 mV_{dif} at I and Q inputs	–	–	2	dB
f_c	output centre frequency		5	–	65	MHz
$Z_{o(dif)}$	differential output impedance		–	150	–	Ω
IP_3	3rd order interception point at I input	see Fig.4	–	–	52	dBmV
H_2	2nd order harmonic of 5 to 65 MHz signal	f = 10 to 130 MHz; V_i = 100 mV_{dif} at I and Q inputs	–	–	–40	dBc
H_3	3rd order harmonic of 5 to 65 MHz signal	f = 15 to 195 MHz; V_i = 100 mV_{dif} at I and Q inputs	–	–	–40	dBc
S_O	mixer spurious outputs of 5 to 65 MHz signal	f = 5 to 65 MHz; V_i = 100 mV_{dif} at I and Q inputs	–	–	–45	dBc
Converter VCO						
$f_{osc(min)}$	minimum oscillation frequency		–	–	145	MHz
$f_{osc(max)}$	maximum oscillation frequency		205	–	–	MHz

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Programmable gain and output buffer; note 1						
$Z_{i(dif)}$	differential input impedance		–	5.6	–	kΩ
ΔG	output level step size		–	–	2	dB
Δbuf_O	output level adjust range	V_i = 30 dBmV sine wave 65 MHz at pins RF_IN and RF_INC; DAC = 0 to 31	32	39	–	dB
V_o	operational output level		–	55	–	dBmV
ΔV_o	output flatness	f = 5 to 65 MHz; V_i = 30 dBmV sine wave; DAC = 28	–	3	5	dB
$V_{IL(ENL)}$	output controlled enable low	output buffer on	–	–	0.8	V
$V_{IH(ENH)}$	output controlled enable high	output buffer off	2.4	–	–	V
ISO	disable isolation	V_i = 100 mV_{dif}; DAC = 28; f = 65 MHz; OE = 0,5 V	–35	–90	–	dBc
$G_{V(max)}$	maximum gain	see Fig.5	17	18.5	–	dB
$V_{o(1dB)}$	1 dB compression point	see Fig.5	58	–	–	dBmV
H_2	2nd order harmonic of 5 to 65 MHz signal	f = 10 to 65 MHz; see Fig.6	–	–	–45	dBc
		f = 65 to 120 MHz; see Fig.6	–	–	–35	dBc
H_3	3rd order harmonic of 5 to 65 MHz signal	f = 15 to 65 MHz; see Fig.6	–	–	–45	dBc
		f = 65 to 120 MHz; see Fig.6	–	–	–35	dBc
Overall; note 1						
Φ_{osc}	phase noise	at 10 kHz; note 2	–	–75	–	dBc/Hz
		at 100 kHz; note 2	–	–95	–	dBc/Hz
H_2	2nd order harmonic of 5 to 65 MHz signal	f = 10 to 130 MHz; V_{in} = 100 mV_{dif} at I and Q inputs; V_{out} = 55 dBmV	–	–	–40	dBc
H_3	3rd order harmonic of 5 to 65 MHz signal	f = 15 to 195 MHz; V_{in} = 100 mV_{dif} at I and Q inputs; V_{out} = 55 dBmV	–	–	–40	dBc
S_o	spurious signals of 5 to 65 MHz signal	f = 5 to 65 MHz; V_{in} = 100 mV_{dif} at I and Q inputs; V_{out} = 55 dBmV	–	–	–45	dBc
IP_3	3rd order interception point at I input		–	–	49	dBmV
ISO_{tot}	total isolation at I/Q midrange	see Fig.7	–	–90	–65	dBc
C/N	carrier to noise ratio at final output at 2 MHz from carrier	V_{in} = 100 mV_{dif}; V_{out} = 35 to 55 dBmV; f = 65 MHz	–	113	–	dBc/Hz

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Crystal oscillator						
f_{xtal}	crystal frequency	note 3	1	–	4	MHz
Z_i	input impedance	f_{xtal} = 4 MHz	600	1200	–	Ω
$V_{i(DC)}$	DC input level		–	2.9	–	V
Modulator synthesizer						
$f_{ref(mod)}$	reference frequency		–	250	–	kHz
RDR1	programmable reference divider ratio		4	–	16	
ND1	fix main divider ratio		–	1120	–	
$I_{(cp)}$	charge-pump current	fixed	–	0.30	–	mA
Converter synthesizer						
f_{step}	step size		100	–	500	kHz
RD2	fix reference divider ratio		–	2	–	
RDR2	programmable reference divider ratio	see Tables 4 and 5	4	–	160	
ND2	fix main divider ratio		–	4	–	
NDR2	programmable main divider ratio	see Tables 4 and 5	290	–	1800	
3-wire bus						
V_{IL}	input LOW level		–	–	0.8	V
V_{IH}	input HIGH level		2.4	–	–	V
Lock detect pin						
$V_{O(lock)}$	output voltage (LOCK)		–	5	–	V
$V_{O(unlock)}$	output voltage (UNLOCK)		–	0.02	–	V
Serial control clock						
f_{clk}	clock frequency		–	330	–	kHz
t_{su}	input data to CLK set-up time	see Fig.8	–	2	–	µs
$t_{h(CLK)}$	input data to CLK hold time	see Fig.8	–	1	–	µs
$t_{d(strt)}$	delay to rising clock edge	see Fig.8	–	3	–	µs
$t_{d(stp)}$	delay from last clock edge	see Fig.8	–	3	–	µs

Notes

1. All specification points of the output section and the overall circuit are measured after the 2 : 1 transformer (Siemens V944) loaded with 75 Ω.
2. Overall phase noise:
   a) Converter: $I_{(cp)}$ = 0.36 mA; f_{ref} = 25 kHz.
   b) I and Q = 100 mV_{dif}.
   c) DAC = 28.
   d) f = 65 MHz.
3. The crystal oscillator uses a 4, 2 or 1 MHz crystal in series with a capacitor. The crystal is serial resonant with a load capacitance of 18 to 20 pF. The connection to V_{CC} is preferred but it might also be to GND.

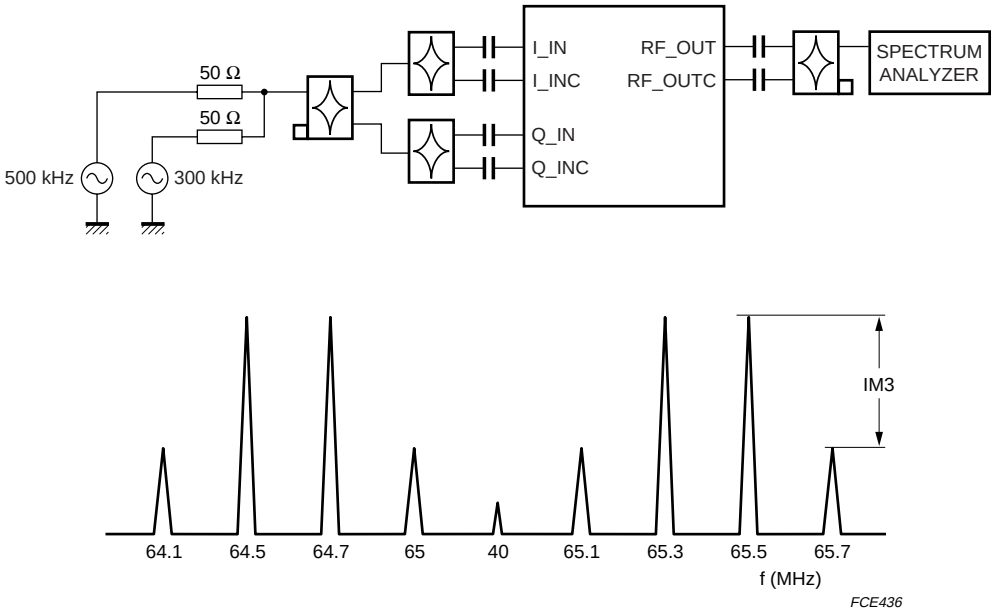


The amplitude imbalance and the LO suppression are measured in the spectrum of the signal measured at the output IF_FILT and are defined in the following conditions:

measure 1: I input frequency = 500 kHz; I input level = 400 mV (p-p) sine wave; unused input as 0 V differential.

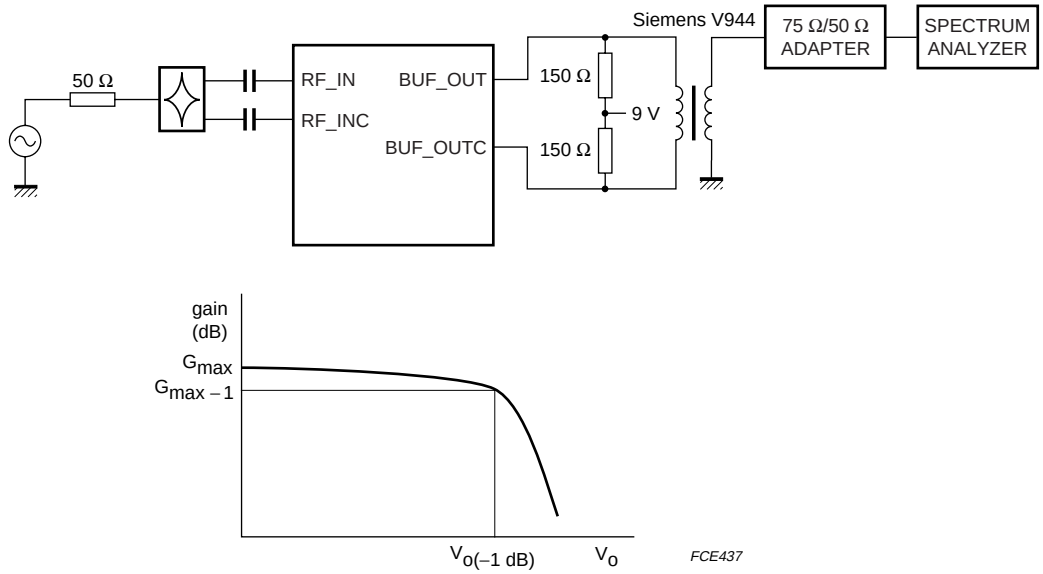
measure 2: Q input frequency = 500 kHz; Q input level = 400 mV (p-p) sine wave; unused input as 0 V differential.

Fig.3 Imbalance and LO suppression.



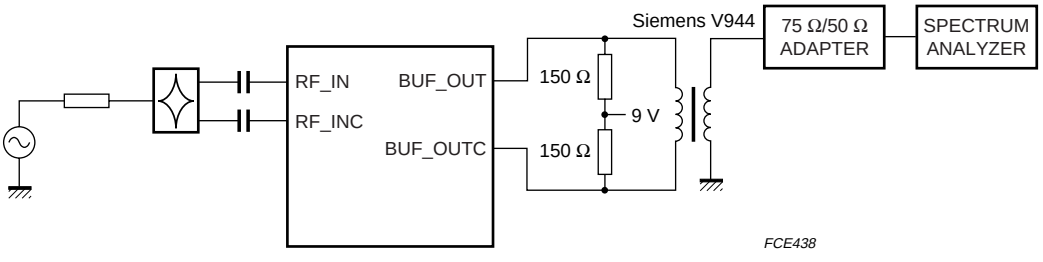
f1 = 300 kHz, f2 = 500 kHz and f_{rf} = 65 MHz.

Fig.4 IP3 set-up measurement.



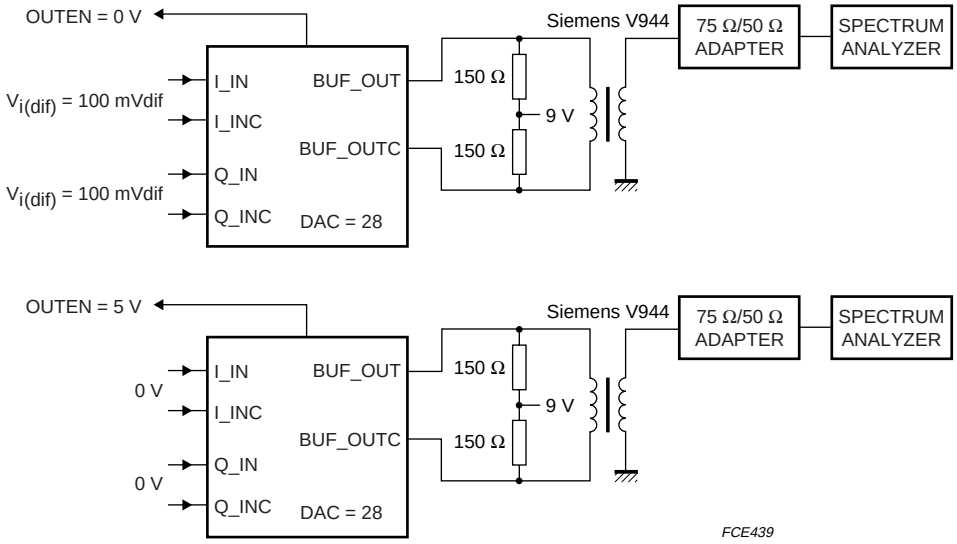
DAC = 31.
f = 65 MHz.
V_i variable to have a variable output voltage.

Fig.5 Maximum gain and compression point.



DAC = 28.
f = 5 to 65 MHz.
V_i such that V_o = 55 dBmV (rms) at 5 MHz.

Fig.6 Harmonics of output sections H2 and H3.



$ISO_{tot} = V_{out1(dB)} - V_{out2(dB)}$.
f_{rf} = 65 MHz.

Fig.7 Total isolation (ISO_{tot}).

APPLICATION INFORMATION

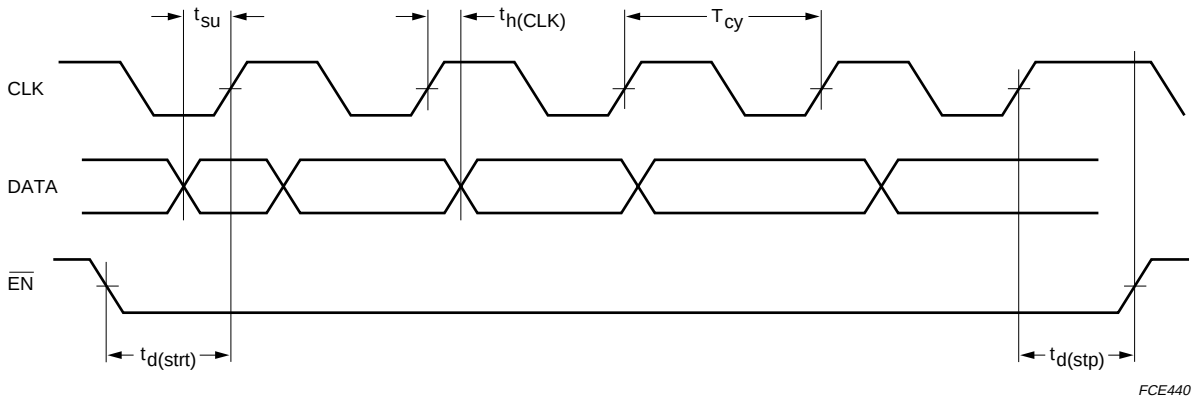


Fig.8 3-wire bus timing.

Table 1 Data format; note 1

DATA												ADDRESS	
D11 first in	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	AD1	AD0 last in
Modulator reference divider ratio				**Converter reference divider ratio**									
X	X	MP1(2)	MP0(2)	R7	R6	R5	R4	R3	R2	R1	R0	0	1
Control register													
X	X	X	OEN(3)	CR2(4)	CR1	CR0(4)	DAC4(5)	DAC3	DAC2	DAC1	DAC0	1	0
Main divider ratio													
P11	P10	P9	P8	P7	P6	P5	P4	P3	P2	P1	P0	1	1

Notes

1. X = don’t care.
2. MP1 and MPO: modulator reference divider ratio (see Table 2).
3. When OEN (output enable) is at logic 0, output is disabled; at logic 1, output is enabled.
4. CR2 and CRO: converter synthesizer charge pump current (see Table 3).
5. When DAC4 to DAC0 is at logic 0, minimum gain is programmed; at logic 1, maximum gain is programmed.

Table 2 Modulator reference divider ratio

MP1	MP0	PROGRAMMED RATIO
1	1	4
1	0	8
0	1	16

Table 3 Converter synthesizer charge pump current

CR2	CR1	CR0	LOCK_CONV(1)	I_{CP}(mA)
0	0	0	0	1.2
0	0	0	1	0.36
0	0	1	0	0.36
0	0	1	1	0.1
0	1	0	X	0.1
0	1	1	X	0.36
1	0	0	X	1.2

Note

1. LOCK_CONV is an internal signal. When at logic 0, converter PLL is out-of-lock. When at logic 1, converter PLL is in-lock.

Table 4 Converter synthesizer

$f_{comp} = f_{osc}/RD$.

f_{osc}\f_{comp}	25 kHz	50 kHz	125 kHz
1 MHz	40	20	8
4 MHz	160	80	32

Table 5 Converter synthesizer;

ND = 4 f_lo = ND × NDR × f_{comp} = NDR × step.

f_{lo}\step	100 kHz	200 kHz	500 kHz
145 MHz	1450	725	290
205 MHz	2050	1025	410

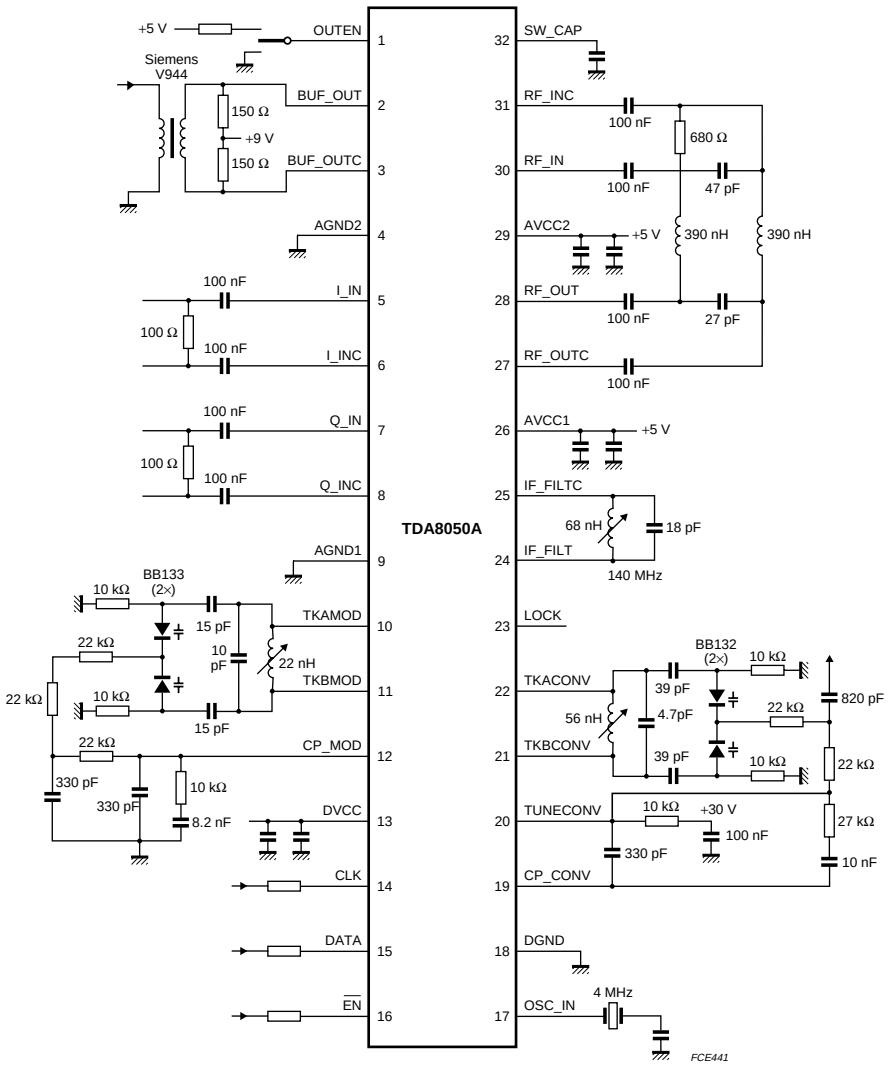
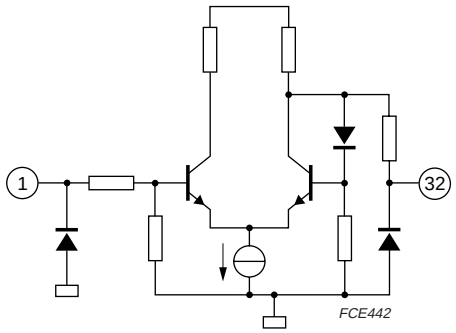
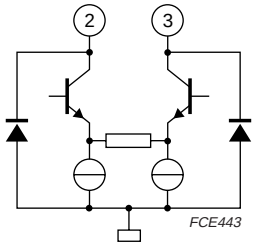
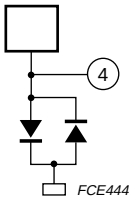
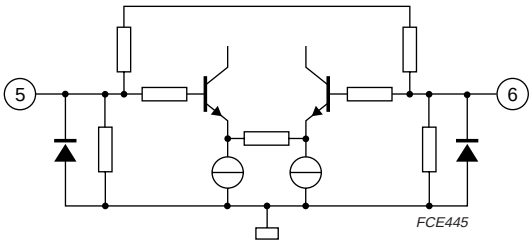
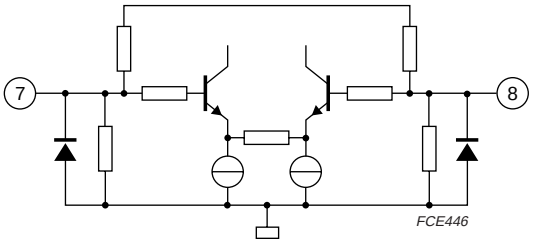
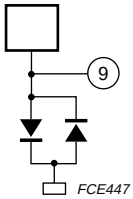
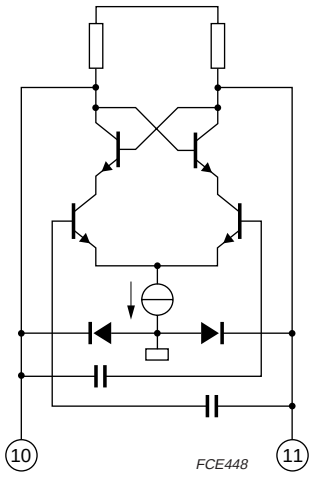
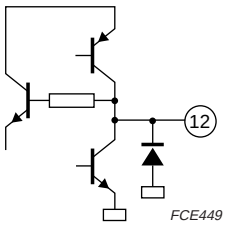
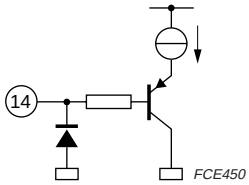
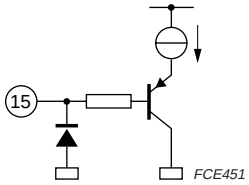
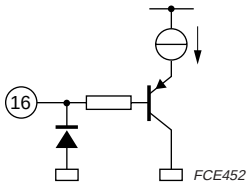
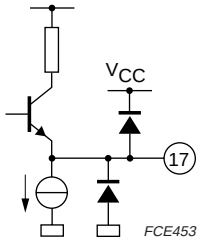
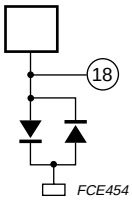


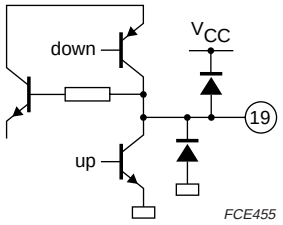
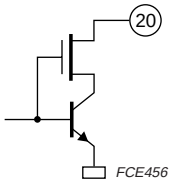
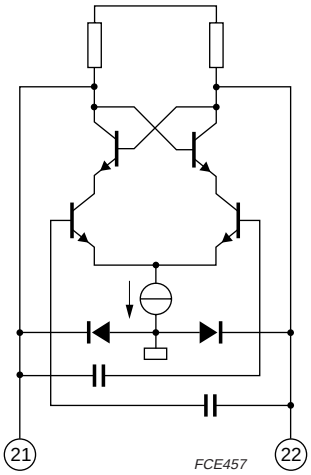
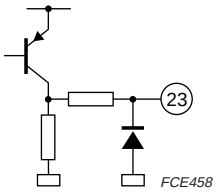
Fig.9 Application diagram.

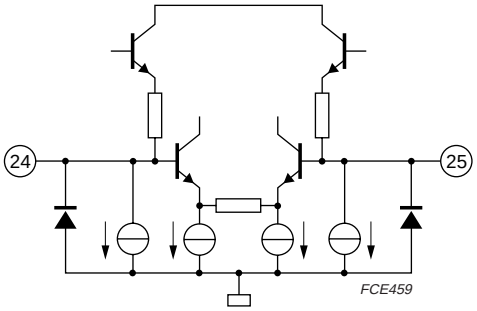
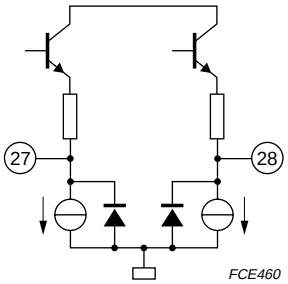
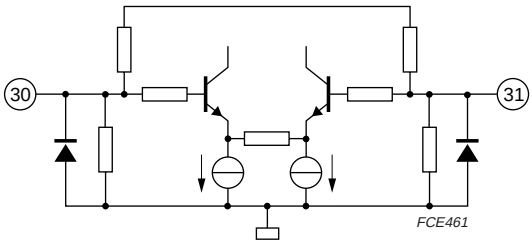
INTERNAL PIN CONFIGURATION

SYMBOL	PIN	DESCRIPTION	DC VOLTAGE
OUTEN SW_CAP	1 32		n.a. 1.7 V
BUF_OUT BUF_OUTC	2 3		5.8 V 5.8 V
AGND2	4		0
I_IN I_INC	5 6		2.5 V 2.5 V

SYMBOL	PIN	DESCRIPTION	DC VOLTAGE
Q_IN Q_INC	7 8		2.5 V 2.5 V
AGND1	9		0
TKA_MOD TKB_MOD	10 11		3.1 V 3.1 V
CP_MOD	12		2.1 V
V_{CCD}	13	supply voltage	5 V

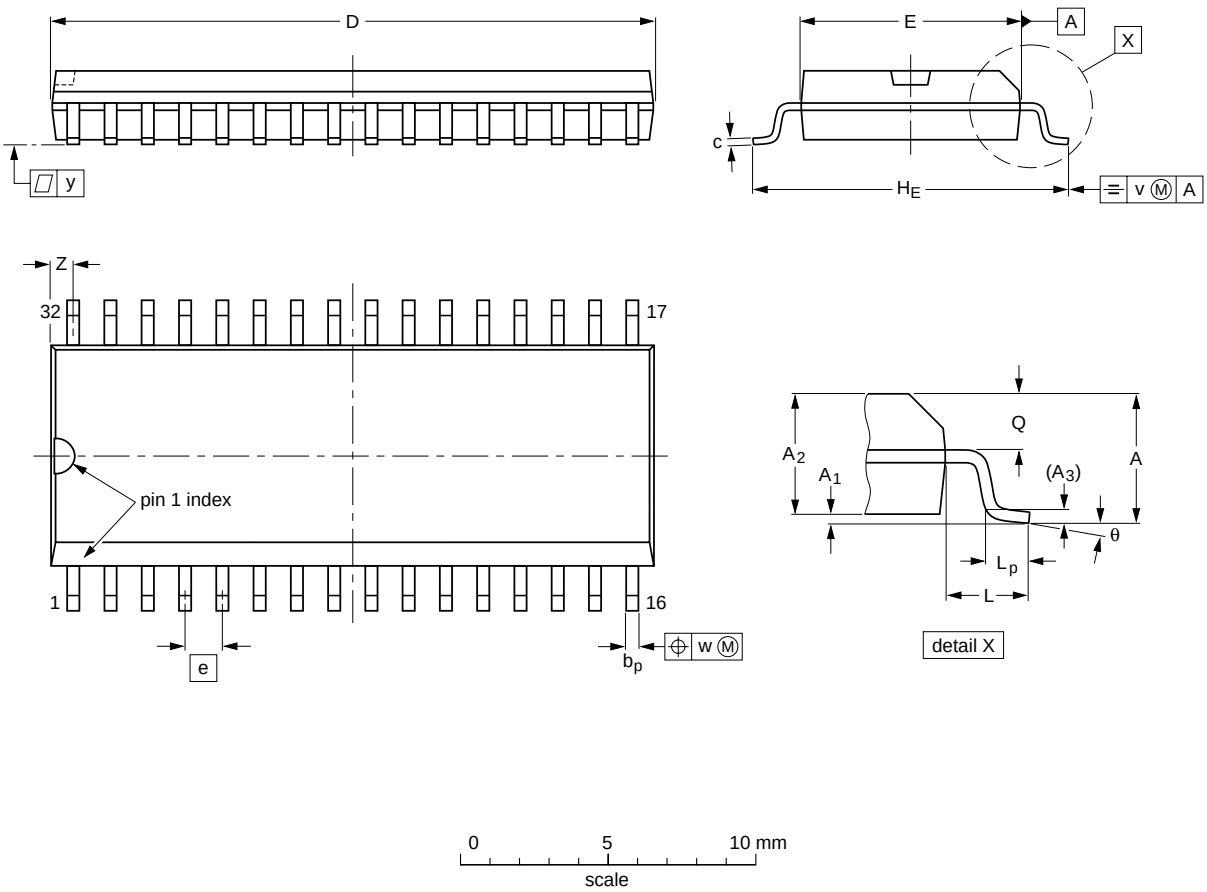
SYMBOL	PIN	DESCRIPTION	DC VOLTAGE
CLK	14		n.a.
DATA	15		n.a.
$\overline{EN}$	16		n.a.
OSC_IN	17		2.9 V
DGND	18		0 V

SYMBOL	PIN	DESCRIPTION	DC VOLTAGE
CP_CONV	19		2.1 V
TUNE_CONV	20		V_{VT}
TKB_CONV TKA_CONV	21 22		3.1 V 3.1 V
LOCK	23		0 V 5 V

SYMBOL	PIN	DESCRIPTION	DC VOLTAGE
IF_FILT IF_FILTC	24 25		2.1 V 2.1 V
V_{CCA1}	26	supply voltage	5 V
RF_OUTC RF_OUT	27 28		3.7 V 3.7 V
V_{CCA2}	29	supply voltage	5 V
RF_IN RF_INC	30 31		2.1 V 2.1 V

PACKAGE OUTLINE

SO32: plastic small outline package; 32 leads; body width 7.5 mm **SOT287-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.27 0.18	20.7 20.3	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.2 1.0	0.25	0.25	0.1	0.95 0.55	8^o 0^o
inches	0.10	0.012 0.004	0.096 0.086	0.01	0.02 0.01	0.011 0.007	0.81 0.80	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.047 0.039	0.01	0.01	0.004	0.037 0.022	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT287-1						~~95-01-25~~ 97-05-22

SOLDERING

Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering is not always suitable for surface mount ICs, or for printed-circuit boards with high population densities. In these situations reflow soldering is often used.

Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 230 °C.

Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE	SOLDERING METHOD	
	WAVE	REFLOW(1)
BGA, SQFP	not suitable	suitable
HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, SMS	not suitable(2)	suitable
PLCC(3), SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended(3)(4)	suitable
SSOP, TSSOP, VSO	not recommended(5)	suitable

Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
2. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
3. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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